5. (Withdrawn) A semiconductor device according to claim 1, wherein the heavy ions are indium ions.

6. (Currently Amended) A method for fabricating a semiconductor device comprising:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask, thereby forming a first ion implanted layer of a second conductivity, at least upper part of which is an amorphous layer;

a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of a first conductivity type; [[and]]

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming an extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and a pocket dopant diffused layer of the second conductivity type, which is in contact with a bottom portion of the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively[[,]];

implanting ions into a surface part of the semiconductor region, thereby forming a fourth ion implanted layer of a second conductivity type before the first step is performed; and

conducting a third annealing process to activate the fourth ion implanted layer, thereby forming a dopant diffused layer to be a shallow channel region,

A.M 1/11/2006

wherein in the second step, a dislocation loop layer is formed in the lower region of the amorphous layer in the semiconductor region due to the heavy ions implantation,
in the fourth step, the pocket dopant diffused layer is formed having a peak dopant concentration produced by trapping heavy ions in the dislocation loop layer, the pocket dopant diffused layer and the extended high-concentration dopant diffused layer are in contact at the peak dopant concentration of the pocket dopant diffused layer, and a side of the extended high-concentration dopant diffused layer, located below the gate electrode, is not